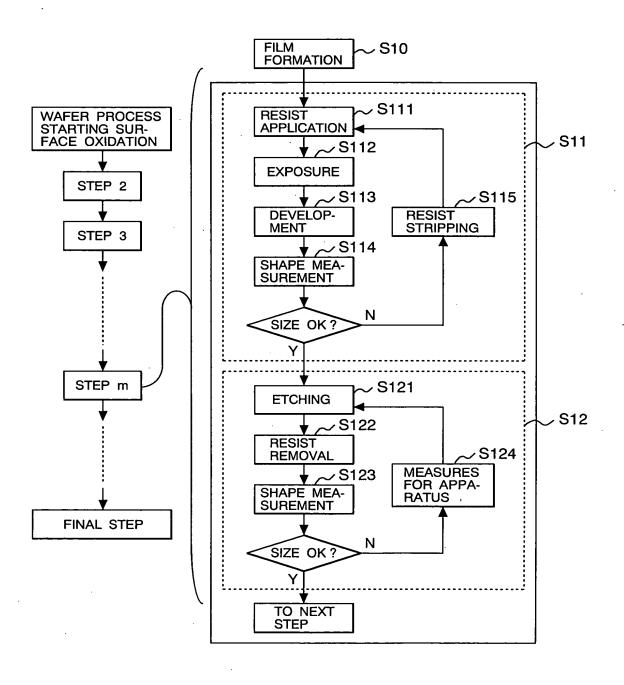
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FIG. 1



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FIG. 2A

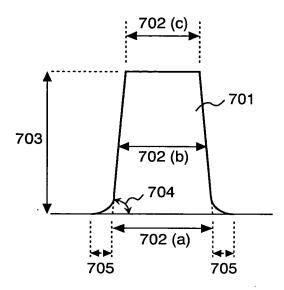
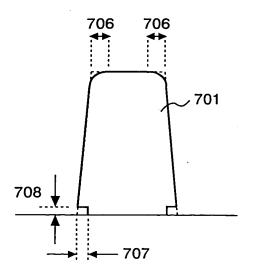


FIG. 2B



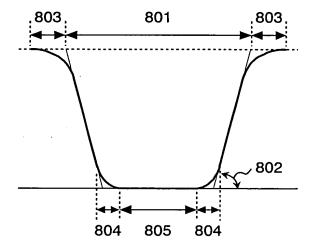
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FIG. 3



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FIG. 4A

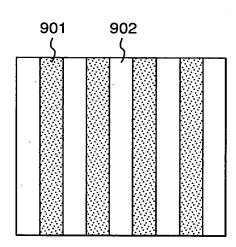


FIG. 4B

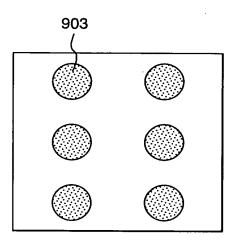
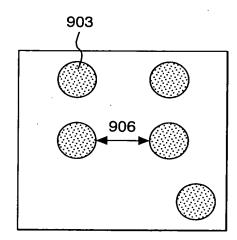


FIG. 4C

901 904 906 905

FIG. 4D



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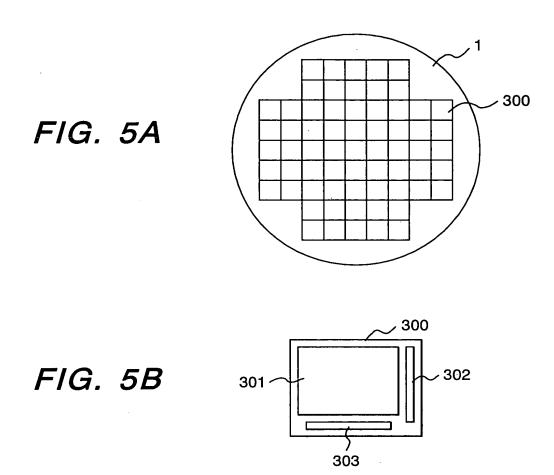
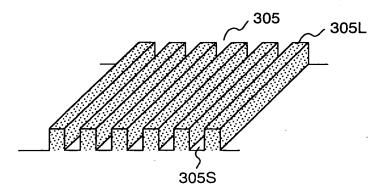


FIG. 6



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FIG. 7

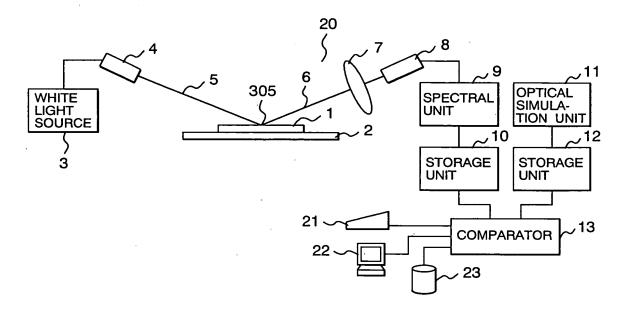
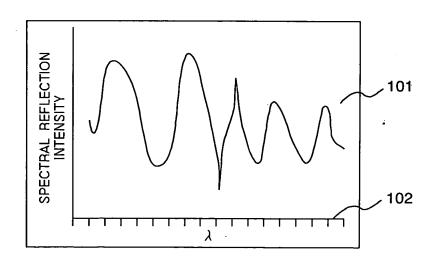


FIG. 8



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FIG. 9

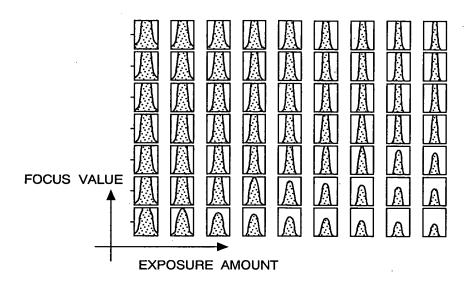
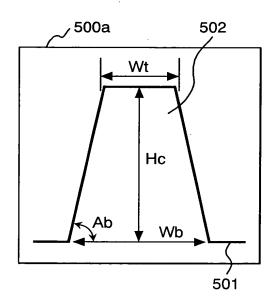
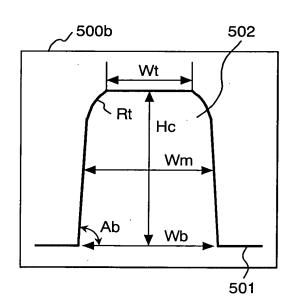


FIG. 10A

FIG. 10B





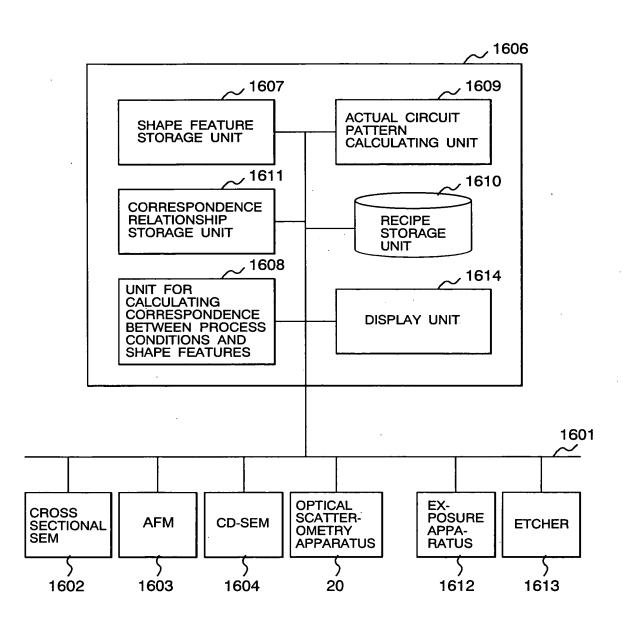
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FIG. 11



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FIG. 12A

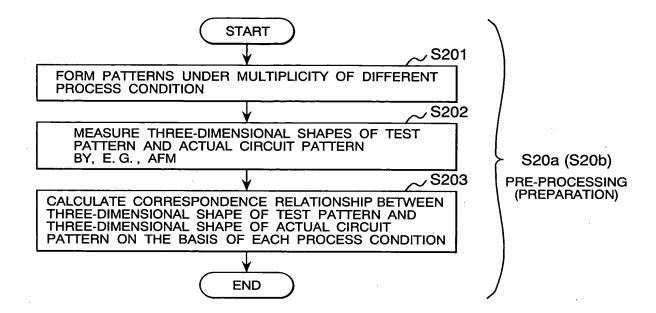
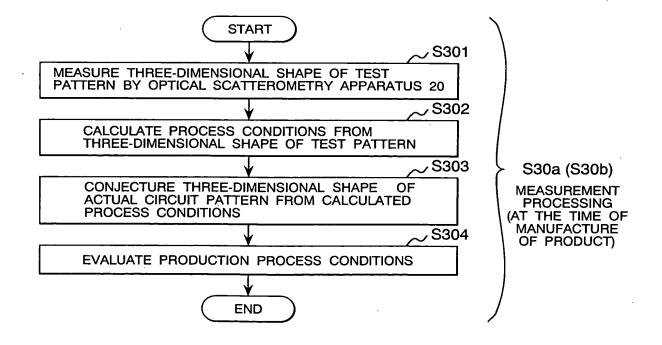


FIG. 12B



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FIG. 13A

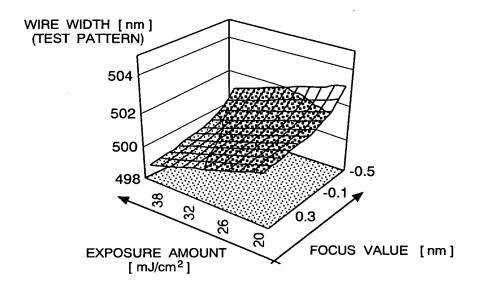
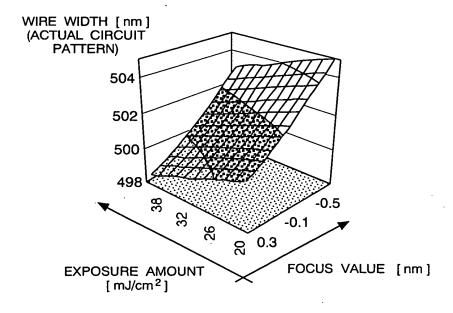


FIG. 13B



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FIG. 14A

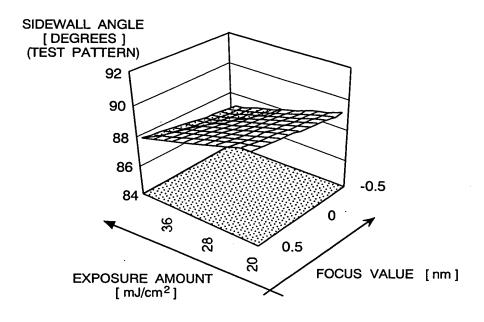
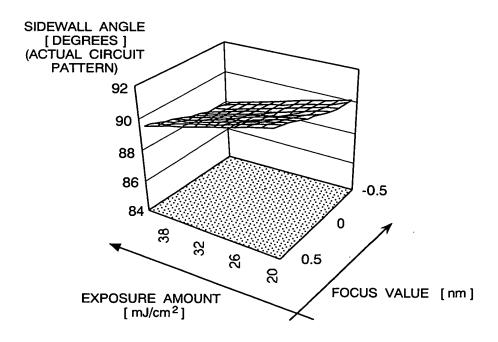


FIG. 14B



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FIG. 15A

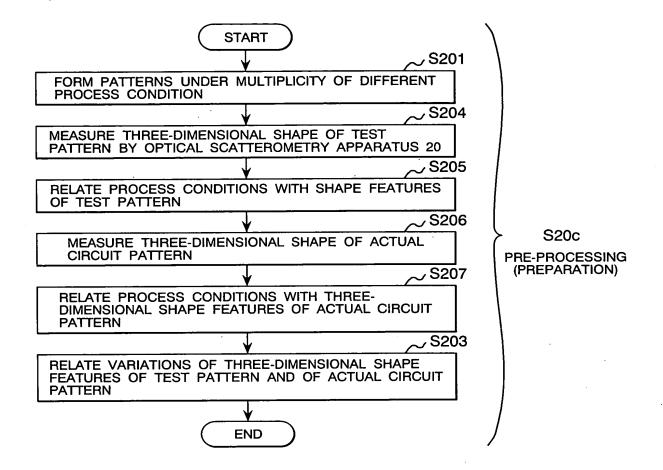
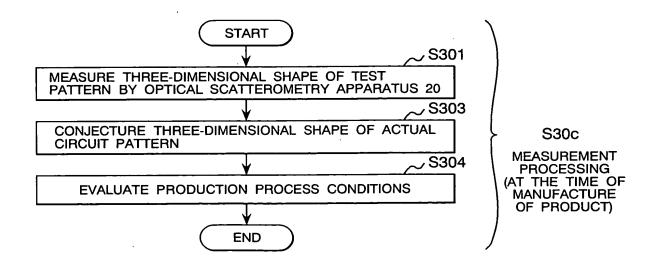


FIG. 15B



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FIG. 16

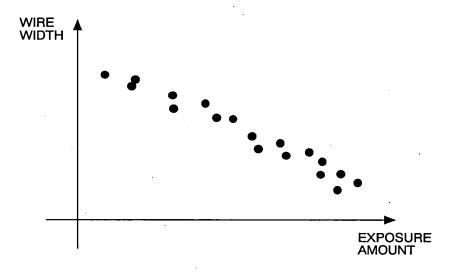
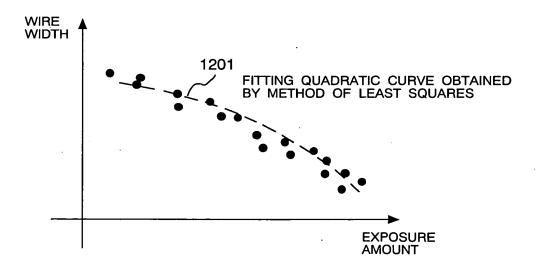


FIG. 17



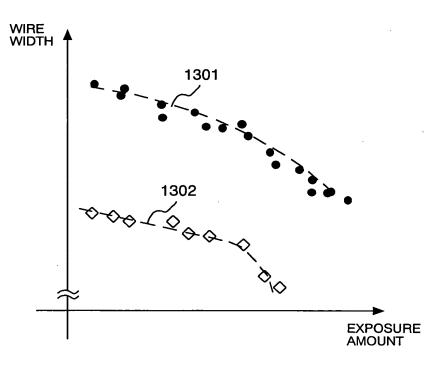
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FIG. 18



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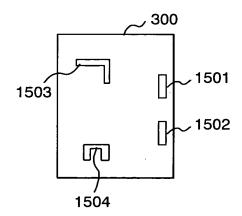
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FIG. 19

#	TEST PATTERN	CRITICAL ACTUAL CIRCUIT PATTERN
1	PATTERN A WIRE WIDTH = F1a (CONDITION1, CONDITION2) SIDEWALL ANGLE = F2a (CONDITION1, CONDITION2)	PATTERN C WIRE WIDTH = F1c (CONDITION1, CONDITION2) SIDEWALL ANGLE = F2c (CONDITION1, CONDITION2)
2	PATTERN B WIRE WIDTH = F1b (CONDITION1, CONDITION2) SIDEWALL ANGLE = F2b (CONDITION1, CONDITION2)	PATTERN D WIRE WIDTH = F1d (CONDITION1, CONDITION2) SIDEWALL ANGLE = F2d (CONDITION1, CONDITION2)

FIG. 20



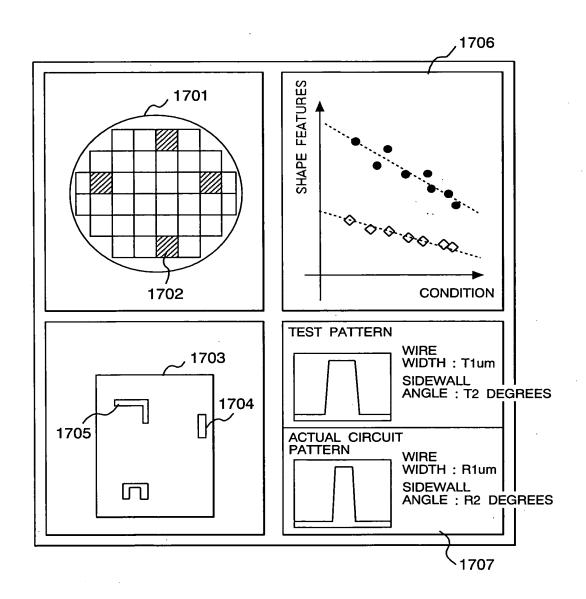
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FIG. 21



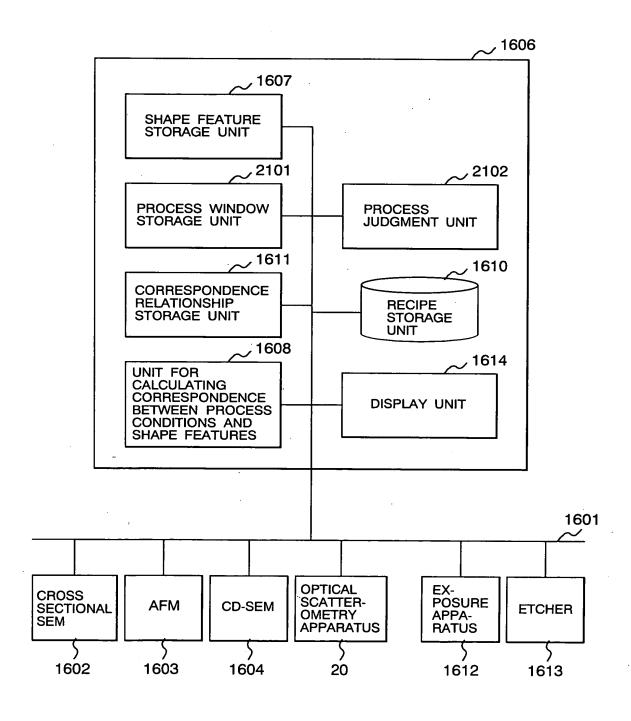
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FIG. 22



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FIG. 23A

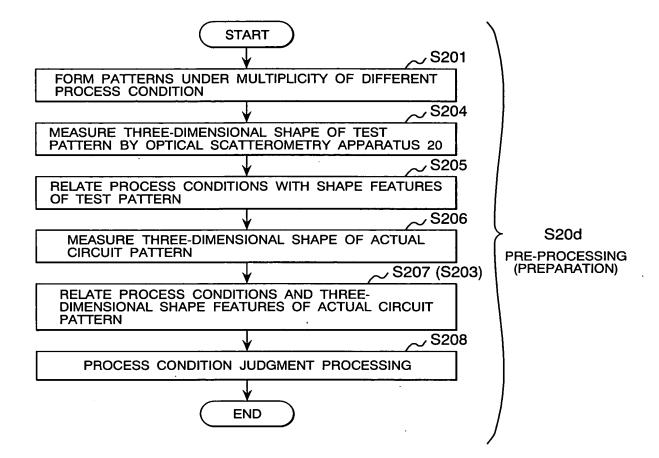
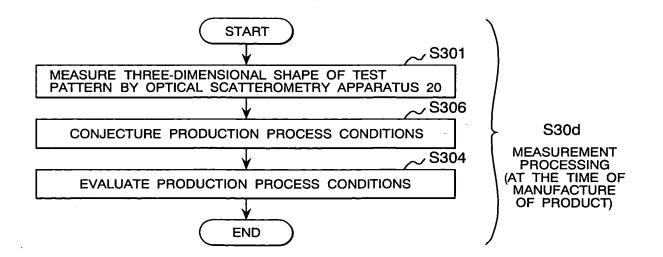


FIG. 23B



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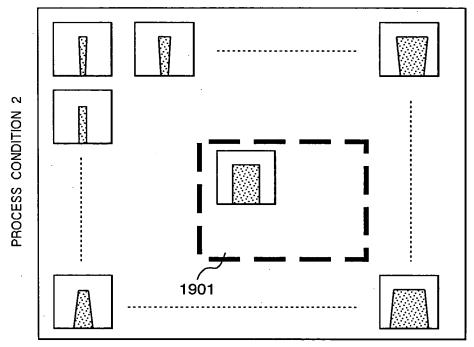
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FIG. 24



PROCESS CONDITION 1

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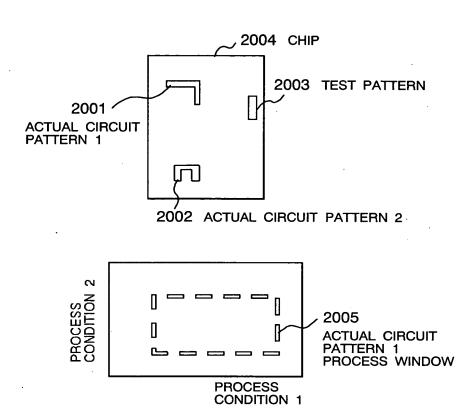
Title: Method and System for Manufacturing Semiconductor Device

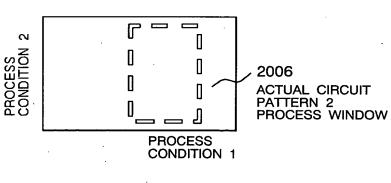
Atty Dock t No. 16869N-099100US

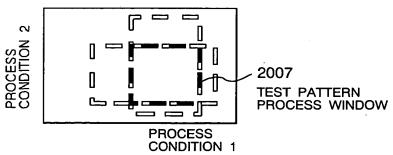
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FIG. 25







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FIG. 26

